A29

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/607,815 | 06/30/2000 | Kenneth W. Batcher | 72255/02662 | 2193 |

23380 7590 12/02/2004

TUCKER, ELLIS & WEST LLP
1150 HUNTINGTON BUILDING
925 EUCLID AVENUE
CLEVELAND, OH 44115-1475

| EXAMINER | |
|---|---|
| HARKNESS, CHARLES A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/607,815 | BATCHER, KENNETH W. | |
| | Examiner | Art Unit | |
| | Charles A Harkness | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Shridhar et al., U.S. Patent Number 5,727,194 (herein referred to as Shridhar).

2. Referring to claims 1 and 8 Shridhar has taught a method of operating a processor to repeatedly execute an instruction;

loading a register with a count value indicative of the number of times the associated instruction is to be executed (Shridhar column 2 lines 20-23 and 31-45, figures 1,3,4 column 13 line 61-column 14 lines 40, column 15 lines 45-49);

fetching and executing a REPEAT instruction, the REPEAT instruction indicating the associated instruction to be repeatedly executed (Shridhar figures 1,3,4 column 13 line 61-column 14 lines 40, column 15 lines 45-49);

fetching the associated instruction (Shridhar figures 1,3,4 column 13 line 61-column 14 lines 40, column 15 lines 45-49); and

repeatedly executing the associated instruction for a consecutive number of times as indicated by the count value (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54).

Without refetching the associated instruction (Shridhar column 2 lines 20-23 and 31-45).

5. Referring to claim 2 Shridhar has taught a method of operating a processor to repeatedly execute a single instruction and to repeatedly execute a block of instructions,

fetching a REPEAT instruction (Shridhar figures 1,3,4 column 13 line 61-column 14 lines 40, column 15 lines 45-49);

executing a REPEAT instruction, wherein execution of the REPEAT instruction stores in a register a count value indicative of the number of tunes an associated instruction is to be executed (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46);

fetching the associated instruction; and

repeatedly executing the single instruction consecutively for as many times as indicated by the count value (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54);

decrementing the count value in the register each time the single instruction is executed (Shridhar column 2 lines 20-23 and 31-45);

incrementing a program counter once the count value in the register is one of less than zero and equal to zero, thereby providing an effective data rate of one transfer every clock cycle (Shridhar column 10 lines 45-53, Table 2 the PC is shown as being stopped while the same instruction is continually fed into the pipeline, but then is advanced once the correct number of iterations of the instruction have been brought into the pipeline to satisfy the repeat count).

6. Referring to claim 3 Shridhar has taught a method of operating a processor to repeatedly execute a single instruction and to repeatedly execute a block of instructions (Shridhar),

loading a register with a count value indicative of the number of times an associated instruction is to be executed (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49);

fetching and executing a REPEAT instruction indicating the associated instruction that is to be repeatedly executed (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49);

incrementing a program counter (Shridhar column 15 lines 9-11 column 16 lines 15-20);

fetching the associated instruction (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49); and

repeatedly executing the associated instruction for as many times as indicated by a count value stored in the count register (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49);

decrementing the count value in the register each time the single instruction is executed (Shridhar column 2 lines 20-23 and 31-45);

stalling the program counter once the count value in the register is one of less than zero and equal to zero, thereby providing an effective data rate of one transfer every clock cycle (Shridhar column 10 lines 45-53, Table 2 the PC is shown as being stopped while the same instruction is continually fed into the pipeline, but then is advanced once the correct number of iterations of the instruction have been brought into the pipeline to satisfy the repeat count).

7. Referring to claim 4 Shridhar has taught wherein said count value is stored in said count register before execution of said REPEAT instruction (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49; since the decode stage come before the fetch stage, as shown in figure 1, the information would be passed in the repeat circuitry before the repeat instruction was executed).

8. Referring to claim 5 Shridhar has taught wherein said REPEAT instruction includes the count value that is stored in said count register, wherein execution of the REPEAT instruction stores the count value in said count register (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49).

9. Referring to claim 6 Shridhar has taught wherein said method further comprises: incrementing the program counter after the associated instruction has been executed for as many times as indicated by the count value (Shridhar column 15 lines 9-11 column 16 lines 15-20 column 18 lines 13-15; the program would have to increment to the next address that it can continue executing the program outside of the loop).

10. Referring to claim 7 Shridhar has taught wherein method further comprises: decrementing said count value stored in said register each time said associated instruction is executed; and determining whether said count value is less than or equal to zero (Shridhar column 18 lines 31-38).

12. Referring to claim 9 Shridhar has taught a processor for repeatedly executing a single instruction and to repeatedly execute a block of instructions,

fetch means for fetching a REPEAT instruction (Shridhar figures 1,3,4 column 13 line 61-column 14 lines 40, column 15 lines 45-49);

execute means for executing a REPEAT instruction, wherein execution of the REPEAT instruction stores in a register a count value indicative of the number of times the instruction is to be executed (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54, Shridhar column 10 lines 45-53);

fetch means for fetching the associated instruction (Shridhar); and

execute means for executing the associated instruction for as many times as indicated by the count value (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54);

means for decrementing the count value in the register each time the single instruction is executed (Shridhar column 2 lines 20-23 and 31-45);

means for incrementing a program counter once the count value in the register is one of less than zero and equal to zero, thereby providing an effective data rate of one transfer every clock cycle (Shridhar column 10 lines 45-53, Table 2 the PC is shown as being stopped while the same instruction is continually fed into the pipeline, but then is advanced once the correct number of iterations of the instruction have been brought into the pipeline to satisfy the repeat count).

13. Referring to claim 10 Shridhar has taught a processor for repeatedly executing a single instruction and to repeatedly execute a block of instructions (Shridhar),

load means for loading a register with a count value indicative of the number of times an instruction is to be executed (Shridhar column 2 lines 20-23 and 31-45);

fetch means for fetching a REPEAT instruction indicating the associated instruction that is to be repeatedly executed; (Shridhar figures 1,3,4 column 13 line 61-column 14 lines 40, column 15 lines 45-49);

execute mean for executing the REPEAT instruction indicating the associated instruction that is to be repeatedly executed (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54);

means for incrementing a program counter (Shridhar column 10 lines 45-53, Table 2);

fetch means for fetching the associated instruction (Shridhar figures 1,3,4 column 13 line 61-column 14 lines 40, column 15 lines 45-49); and

execute means for repeatedly executing the associated instruction for a consecutive number of as indicated by a count value stored in a count register (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54);

means for decrementing the count value in the register each time the single instruction is executed (Shridhar column 2 lines 20-23 and 31-45);

means for incrementing a program counter once the count value in the register is one of less than zero and equal to zero, thereby providing an effective data rate of one transfer every clock cycle (Shridhar column 10 lines 45-53, Table 2 the PC is shown as being stopped while the same instruction is continually fed into the pipeline, but then is advanced once the correct number of iterations of the instruction have been brought into the pipeline to satisfy the repeat count).

14. Referring to claim 11 Shridhar has taught wherein said count value is stored in said count register before execution of said REPEAT instruction (Shridhar column 2 lines 20-23 and 31-45).

15. Referring to claim 12 Shridhar has taught wherein said REPEAT instruction includes the count value that is stored in said count register, wherein execution of the REPEAT instruction stores the count value in said count register (Shridhar column 2 lines 20-23 and 31-45).

16. Referring to claim 13 Shridhar has taught wherein said processor further comprises: means for incrementing the program counter after the associated instruction has been executed for as many times as indicated by the count value (Shridhar column 10 lines 45-53, Table 2 the PC is shown as being stopped while the same instruction is continually fed into the pipeline, but then is advanced once the correct number of iterations of the instruction have been brought into the pipeline to satisfy the repeat count).

17. Referring to claim 14 Shridhar has taught wherein processor further comprises:

means for decrementing said count value stored in said register each time said the instruction is executed; and

means for determining whether said count value is less than or equal to zero (Shridhar column 2 lines 20-23 and 31-45).

18. Referring to claim 15 Shridhar has taught a processor for repeatedly executing a single instruction and to repeatedly execute a block of instructions (Shridhar),

a memory address register associated with a main memory (Shridhar figure 1);

a memory control for generating memory control signals (Shridhar figure 1);

a program counter for storing a memory address location of the main memory where an instruction is to be fetched (Shridhar figure 3);

an instruction register for storing an instruction that is to be executed (Shridhar figure 3 number 166);

at least one general purpose register storing a count (Shridhar column 2 lines 20-23 and 31-45);

decode and execute control logic for decoding and executing an instruction stored in the instruction register (Shridhar figure 3); and

a state machine for controlling the fetching and repeated execution of an associated instruction (Shridhar column 2 lines 20-23 and 31-45);

decrementing the count value in the register each time the single instruction is executed (Shridhar column 2 lines 20-23 and 31-45)

incrementing a program counter once the count value stored in the general purpose register is below a threshold value, thereby providing an effective data rate of one transfer every clock cycle (Shridhar column 10 lines 45-53, Table 2 the PC is shown as being stopped while the same instruction is continually fed into the pipeline, but then is advanced once the correct number of iterations of the instruction have been brought into the pipeline to satisfy the repeat count).

19. Referring to claim 16 Shridhar has taught wherein said processor further comprises an instruction buffer for storing the associated instruction (Shridhar).

21. Referring to claim 17 Shridhar has taught wherein said general purpose register includes a first register for storing a count value indicative of the number of times the one or more associated instructions are to be repeatedly executed (Shridhar column 2 lines 20-23 and 31-45).

21. Referring to claim 18 Shridhar has taught wherein said state machine generates signals for decrementing the count value stored in the first register (Shridhar column 2 lines 20-23 and 31-45).

22. Referring to claim 19 Shridhar has taught wherein said state machine generates a signal for executing an instruction stored in said instruction register (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49).

23. Referring to claim 20 Shridhar has taught wherein said state machine generate a signal for incrementing said program counter after the associated instruction is repeatedly executed (Shridhar column 10 lines 45-53, Table 2 the PC is shown as being stopped while the same instruction is continually fed into the pipeline, but then is advanced once the correct number of iterations of the instruction have been brought into the pipeline to satisfy the repeat count).

Referring to claim 21 Shridhar has taught wherein the means for executing the REPEAT instruction and the means for repeatedly executing the single instruction are the same means (Shridhar figures 1,3,4 column 13 line 61-column 14 lines 40, column 15 lines 45-49).

Referring to claim 22 Shridhar has taught wherein the means for fetching a REPEAT instruction and the means for fetching the single instruction are the same means (Shridhar figures 1,3,4 column 13 line 61-column 14 lines 40, column 15 lines 45-49).

Referring to claims 23 and 26 Shridhar has taught further comprising incrementing the program counter once the count value is equal to zero (Shridhar column 10 lines 45-53, Table 2

the PC is shown as being stopped while the same instruction is continually fed into the pipeline, but then is advanced once the correct number of iterations of the instruction have been brought into the pipeline to satisfy the repeat count).

Referring to claims 24 and 27 Shridhar has taught further comprising incrementing the program counter once the count value is less than zero (Shridhar column 10 lines 45-53, Table 2 the PC is shown as being stopped while the same instruction is continually fed into the pipeline, but then is advanced once the correct number of iterations of the instruction have been brought into the pipeline to satisfy the repeat count).

Referring to claims 25, 28, 29 and 31 Shridhar has taught wherein the program counter remains unchanged as the single instruction is repeatedly executed (Shridhar column 10 lines 45-53, Table 2 the PC is shown as being stopped while the same instruction is continually fed into the pipeline, but then is advanced once the correct number of iterations of the instruction have been brought into the pipeline to satisfy the repeat count).

Referring to claims 30 and 32 Shridhar has taught wherein the program counter is effectively stalled on the single instruction until the single instruction executes the number of times indicated by the count value (Shridhar column 10 lines 45-53, Table 2 the PC is shown as being stopped while the same instruction is continually fed into the pipeline, but then is advanced once the correct number of iterations of the instruction have been brought into the pipeline to satisfy the repeat count).

***Response to Arguments***

Applicant's arguments with respect to claims filed on 08/27/04 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 571-272-4167. The examiner can normally be reached on 9Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Allen Harkness
Examiner
Art Unit 2183
November 23, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100